IN THE SPECIFICATION

Please amend the paragraph beginning on page 4 line 31, as follows:

The aforementioned objects, features and advantages of this invention will become apparent by referring to the following detailed description of a preferred embodiment with reference to the accompanying drawings, wherein:

Fig. 1 is a schematic diagram of a typical FED cathode plate;

Fig. 2 is a diagram of the fabrication steps of Fig. 1;

Fig. 3 is a schematic diagram of an FED cathode plate of the invention;

Fig. 4 is a diagram of the fabrication steps of Fig. 3; ~~and~~

Fig. 5 is a comparison table of the fabrication steps of Figs. 2 and 4 [[.]] ; and

Figs. 6a to 6f are cross sections of the manufacturing process for the FED cathode plate as shown in Fig. 3.

Please amend the paragraph beginning on page 5 line 8, as follows:

As shown in Fig. 3, the FED cathode plate with the internal via has a substrate 10 as the base of deposition. The material of the substrate 10 is glass. The resistive layer 11, a doped layer with a plurality of cathode conductors 13, is implemented over the substrate 10 to prevent a microtip 2 from being formed from excessive current. The material for the cathode conductors is niobium (Nb) . The cathode conductors 13 are etched based on a column pattern to create a column line surrounding the cathode conductors 13. At the same time, the tape line 18 is formed on the substrate 10 maintaining a distance from the resistive layer 11. The tape line 18 is chromium (Cr). The tape line 18 is a thin film deposited along with the path from gate lines 5a and

5b, through a contact 7, bond wiring to a metal pad (not shown) outside. Next, the cathode is joined and sealed to the anode 9 with an adhesive 8, e.g. glass frit, thereby producing an electrode. The electrode interacts with the outside through the thin film 18. The first dielectric layer 16a formed of SiO_2 is located on the resistive layer 11 and part of the tape line 18 and has microtip cavities 3 to accommodate microtips 2. Dry etching the first dielectric layer 16a forms the cavity 3, about 2 μm wide. The first dielectric layer 16a acts as an insulator. The first gate line 5a is located on the first dielectric layer 16a in order to use the first dielectric layer 16a to prevent the first gate line 5a from directly contacting the cathode conductors 13. The material for the gate line is niobium (Nb). The first gate line 5a has a respective hole 4 located at the microtip 2. The hole 4 is deposited to be a diameter about 1.6 μm wide. The internal via 6 is located on the tape line 18 and abutted against the first dielectric layer 16a and the gate line 5a. The internal via 6 is formed by dry etching. The second dielectric layer 16b is located on the tape line and abutted against the internal via 6. The first dielectric layer 16a and the second dielectric layer 16b have the same height and is ~~Nb~~ SiO_2. The adhesive 8, for example, glass frit, is used to connect the second dielectric layer 16b of the cathode to an anode 9. The second gate line 5b is located on the second dielectric layer 16b and abutted against the internal via 6. The first gate line 5a is the same height as the second gate line. The metal layer is covered over the first gate line 5a, the internal via 6, and ~~the metal layer 12 of~~ the second gate line 5b. The metal layer 12 is about 2000 Å and is formed of niobium (Nb) . The contact 7 is located on the tape line 18 and connected adjacent to the second dielectric layer 16b, thereby electrically connecting a lead (not shown) to the outside through the internal via 6 and the tape line 18.

Please amend the paragraph beginning on page 7 line 3, as follows:

As shown in Fig. 4, in steps S41 and S42, the detail is shown in Fig. 5 that layers except for the substrate 10 are in the comparison table. Figs. 6a to 6f are cross sections of the manufacturing process for the FED cathode plate as shown in Fig. 3. ~~As shown in~~ In Fig. [[5]] 6a, for the novel part concurrently referring to Fig. 3, ~~the first~~ a layer [[is]] such as an Nb-including metal layer [[,]] is deposited to form ~~the column line 15~~ a plurality of cathode conductors 13 and the tape line 18. In Fig. 6b, a resistive layer 11 is formed to cover the cathode conductors 13 and maintain a distance from the tape line 18. The ~~second~~ resistive layer 11 is a [[the]] doped-silicon resistive layer [[11]] having the resistance function. In Fig. 6c, ~~The third~~ a dielectric layer 16 and a gate line 5 is formed on the resistive layer 11 and the tape line 18. In Fig. 6d, the dielectric layer 16 and a gate line 5 is etched to form [[the]] a microtip cavity 3, a hole 4, [[the]] an internal via 6, and a contact 7. ~~The fourth layer is gate lines 5a and 5b.~~ Thus, the invention deposits [[an]] a FED cathode structure from bottom to top including a substrate, a resistive layer, a dielectric layer and a gate line. Also, the invention uses dry etching in the cathode structure to form a cathode plate with the hole and the microtip cavity ~~of a microtip~~, an internal via, and a contact. ~~The microtip is molybdenum.~~ In ~~step S43~~ Fig. 6e, the plate is sloped to a predetermined angle in order to form a metal layer on the gate line and the internal via contacting with the tape line by evaporation. The predetermined angle is preferably between 10 and 30 degrees. The material for evaporation to form the metal layer is Nb, compared to Al in the prior art. In ~~step S44~~ Fig. 6f, the plate is recovered in a horizontal direction with the face to be deposited downward, thereby forming a microtip 2 within the microtip cavity 3. The microtip 2 is molybdenum. Sequentially ~~In step S45~~, excessive deposition on the surface of the plate is removed by solution, e.g. phosphoric acid and

the Nb-including metal layer 12 and the microtip 2 are retained. [[The]] Finally, referring to Fig. 3, the completed cathode plate is joined and sealed with the anode 9 by adhesive 8, e.g. glass frit. [[An]] A FED is thus completed.

IN THE DRAWINGS

Applicant respectfully presents herewith replacement Figure 3 and new Figures 6a, 6b, 6c, 6d, 6e and 6f, which include the desired changes, without markings, and which comply with 37 C.F.R. §1.84.